Ultra shallow junction doping by high density inductively coupled plasma for 3D devices structures

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Abstract

Advanced inductively coupled plasma techniques and surface treatments have been used to demonstrate 5 nm conformal shallow junctions at low energy with no silicon structure damage. N-type PH_3 plasma assisted doping was characterized by dopant diffusion and electrical activation with increasing wafer temperature. Plasma assisted doping at high wafer temperature showed no structure damage even at a high incident energy condition with a bias power applied to the wafer, while a shallow junction of less than 7 nm of Xj formation was achieved with low incident energy condition without bias power. Adding a silicon surface modification step when using the decoupled plasma condition prior to PH_3 doping was found to enhance the dopant level and lower Rs dramatically. Various annealing techniques were compared to understand the impact to dopant activation and levels to form shallow junctions of less than 7 nm.

1. Introduction

Increasing demands for information technology (IT) are driving demand for high density memory and logic. To meet these demands and to continue scaling, 3D structures have been introduced in NAND and logic FEOL[1.2)]. Based on device technology roadmaps, shallow junction depths of less than 10 nm are required for the less than 14 nm node logic[3)] device, therefore, various doping techniques have been considered to meet the requirement shown in Figure 1.

Conventional beam-line ion implantation has challenges forming shallow junctions conformally in high aspect ratio features, such as 20 nm FinFET. The primary limitation with conventional beamline implantation of 3D structures is related with the directionality of ions. As shown in Figure 2, the pitch of fin arrays is too small to inject ions on the sidewall surface

with uniform depth control. Ion implantation involves both ions shading and penetrating the surface at the same time as ions traverse with fixed incident angle. This results in a non-uniform doping depth on the fin sidewall, leading to unreliable source/drain current.

Plasma doping using high density plasma reactors such as hollow cathode or inductively coupled plasma (ICP) has demonstrated the formation of shallow junction by low energy (<500 eV) with high dose for fabricating ultra-shallow junctions[4]. It can be used effectively on high aspect ratio features with ion directionality control [5]. However, even though plasma doping appears to be a promising technology, it has experienced limited utilization in critical applications[6]. The stringent requirements for controllability of junction depth on 3D structures, requires alternative approaches such as mono-layer doping technologies including atomic layer deposition (ALD)[7,8], spin-on[9], gas phase[10], and optimized plasma doping[11, 12].

As the scaling down of MOS devices continues, ultra shallow S/D junction depth is required to reduce the short channel effect and to increase the device performance. Plasma doping technology has been developed due to its high dose capability with low ion energy, high activation efficiency, doping profile control and relatively low damage over beamline implantation. However, concern over incident ions direction control has limited its use in the formation of shallow junctions with uniform doping on 3D structure such as FinFET, since plasma doping often uses bias power to generate enough ion energy to implant ions and increase dopant levels at the Si substrate. As shown in Figure 3, even though plasma doping could minimize the depth penetration of ions by reducing ion energy, it is difficult to fully avoid the issue of directionality due to its sheath on the wafer surface.

It has been suggested broadly that adding dopants on the silicon surface to form the ultra-shallow junction after activating and driving in the dopant thermally is an alternate method to plasma doping due to its simplicity and expectation of no structural damage on the surface during process[13]. In this approach, the dopant atoms are deposited on the silicon surface through the thermal decomposition of either solid or gaseous precursors such as B_2H_6, PH_3 and AsH_3.

2. Experimental and Discussion

The apparatus, which is an inductively coupled plasma reactor to control plasma density and ions energy independently to generate ions and radicals uniformly across the wafer and

implant them into the target surface, is shown in Figure 4. The electrostatic chuck (ESC) holds the wafer with He on backside to maintain wafer temperature.

A PH_3 based plasma process has been used to dope P into (100) oriented p-type Si with low energy and high dose condition. Various forms of annealing including RTP, laser, and flash were evaluated to activate dopants electrically, and sheet resistance (*Rs*) was confirmed by 4-point probe (4pt-pb). Impurity profiles and dose were measured by both SIMS and TEM for both blanket and structure wafers, respectively. And spreading resistivity profile (SRP) was used to confirm the electrical activation levels in addition to *Rs*.

Ultra-shallow junction doping was evaluated by performing the plasma doping process on 3D Si structures. The main issue with plasma doping at nano--scaled 3D structure such as FinFET is corner erosion by ions bombardment caused by the sheath depth during doping process and its dopant depth uniformity, i.e., conformality [14].

Figure 5 is a TEM comparison of a silicon fin structure with and without plasma doping. Both samples have been annealed with RTP after an ALD SiN film was deposited in-situ without vacuum break after the plasma process to compare the performance of plasma doping on structure. Since the doping process does not contain bias power to accelerate ions to wafer, minimal impact on Si surface is obtained. Finally the junction depth and dopant slope can be controlled by various annealing conditions including RTP, flash, and laser as shown in Figure 6, and further optimization may reduce the junction to less than 5 nm.

3. Conclusion

In summary, we have performed plasma assisted doping to form ultra-shallow junction on 3D structure. The dopants and their activation level can be increased by adding surface treatments which increase the vacancies between Si-Si to embrace more dopants. No erosion on the corner of the topographical structure after plasma doping process has been observed, since the process condition has no bias power to avoid the energetic ions bombardment. Optimization of annealing produces less than 5 nm junction depth.

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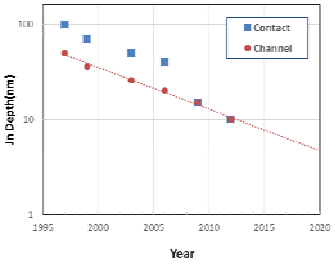

Fig. 1: For comparison, an industry target by ITRS on device junction depth is shown for both channel and contact [3] .

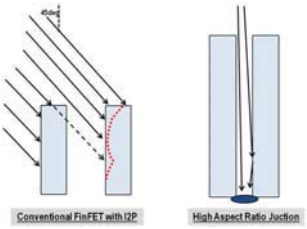

Figure 2: a) Beamline implantation generates a non-uniform depth profile on FinFET channel due to ion shading and penetrating. b) Control of ion beam incident angle with multiple doses to form shallow junctions is a challenge in HAR features.

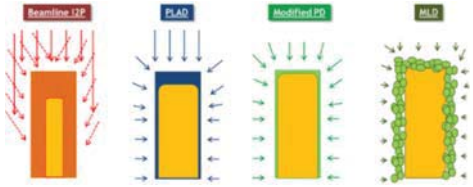

Figure 3: Illustration of expected dopant distribution by various doping techniques. (from left, conventional I^2P, conventional plasma doping, modified plasma assisted doping, and mono-layer doping, respectively)

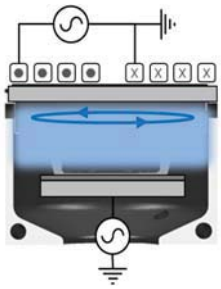

Figure 4: High density plasma sources to generate ions uniformly across the wafer are shown.

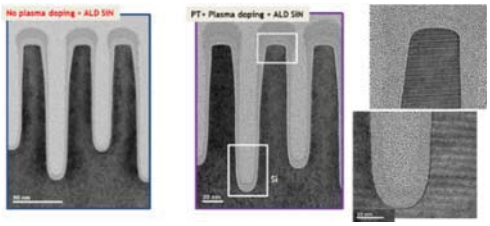

Figure 5: TEM of post annealed sample with 3D structure without (left) and with (right) plasma doping process. No difference on the corner shape of the top of Si fin is seen between two samples. More detail TEM (far right) shows no faults in the Si structure.

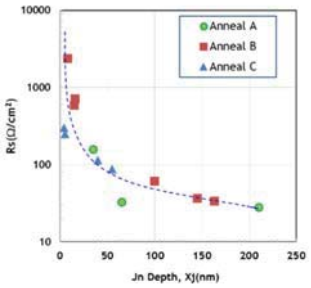

Figure 6: Various annealing techniques produces different performance on junction depth (X_j)